CME EMB with AHB interface

(tdp mode)

Design Example

User Guide

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Contents

1 Introduction

This document describes an example that uses ARM to access the AHB interface EMB on FPGA. Following is the detail of the example:

- Function
  - In the example, the EMB(tdp) with AHB interface module works as slave of AHB Bus and whose port A connect with the AHB slave interface port.
  - ARM writes data to the EMB port A. In the case, ARM gives the data and address that fit the AHB bus.
  - FPGA logic accesses the corresponding address and read the data from the EMB port B and compare the read data to make sure whether the results are correct.
  - FPGA logic writes to the EMB port B when read is finished.
  - ARM accesses the EMB port A to read the data and compare the read data.
  - DMA transfer data from SRAM/EMB to EMB/SRAM and compare the data.
  - The compared results and read/write status are printed on PC through serial port.
- The example works at
  - FPGA Array logic: 50MHz
  - ARM core: 200MHz
- Device: CME-M7
- Test board: CME-M7-EVB-V1.3(2014-06-03)

2 System Level Structure

The general structure of this example as follows:

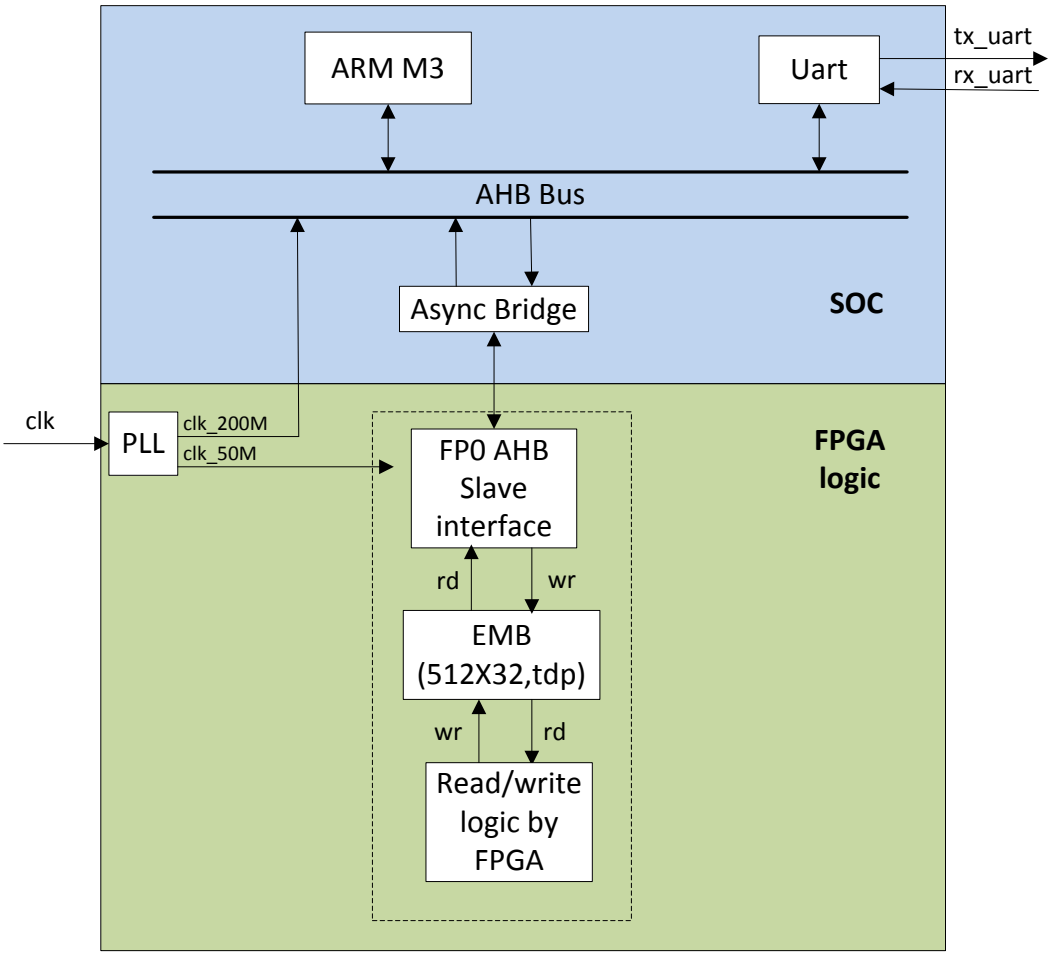

Figure 2-1 ***System level structure of the example***

This case consists of 4 parts as is shown in the above figure: PLL, SOC/ARM, EMB_AHB(512x32), FP logic(access port B).

1. PLL(generated by Wizard):
   a) This part has an input of 20MHz and provides the clock 200MHz and 50MHz,the former is used by ARM and the latter is used in FPGA logic.
   The block can be configured as the figure 2-2 below in the Primace software by Wizard tool.
   In the setting parameters, PLL location is set ''2''.

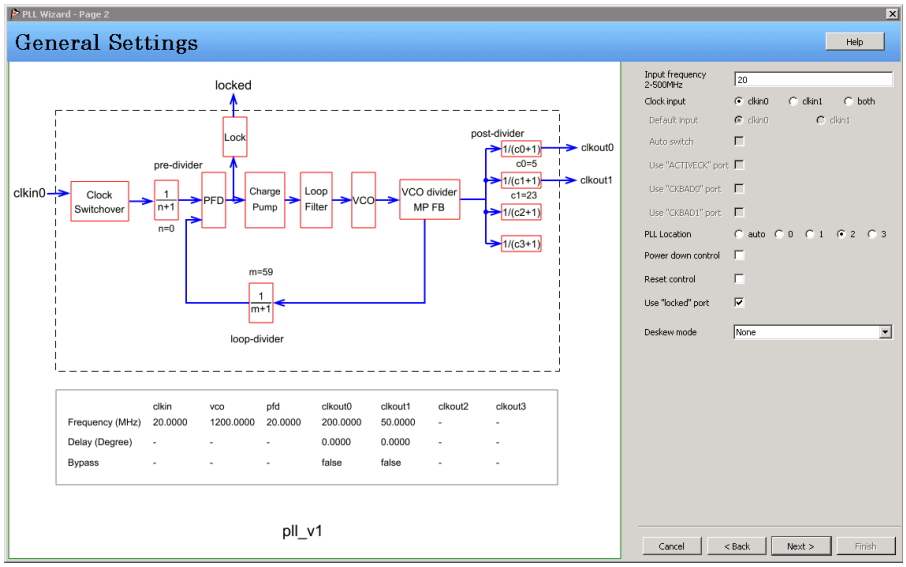

Figure 2-2 ***PLL block configuration***

2. SOC/ARM(generated by Wizard):

   a) This part is an ARM M3 processor core, which contains some hard peripherals. In the example, a UART2 peripheral and an GPIO are used and FPGA logic connects with the AHB0 slave interface.

   b) It is configured as the figure 2-3(a),2-3(b),2-3(c).

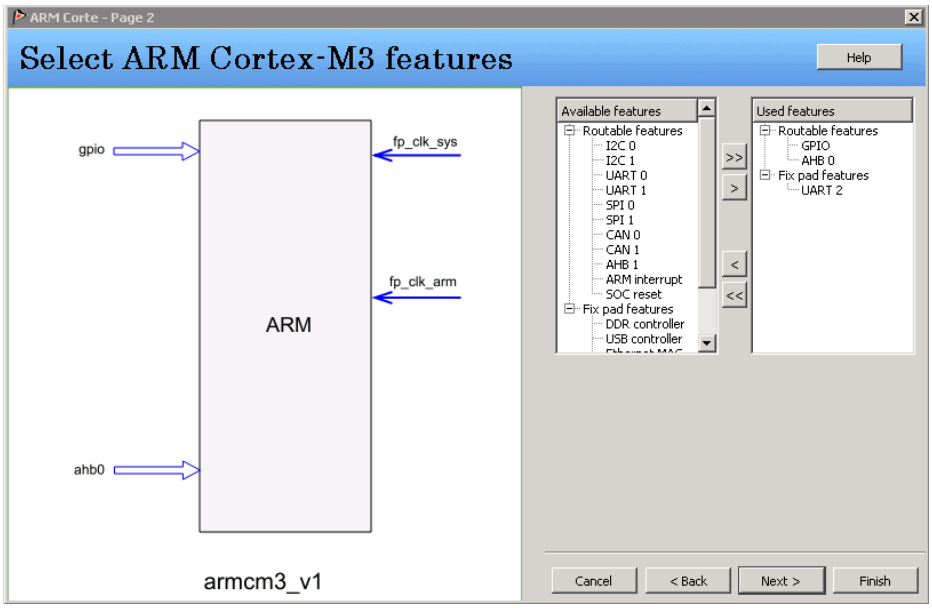

Figure 2-3(a) ***select peripherals***

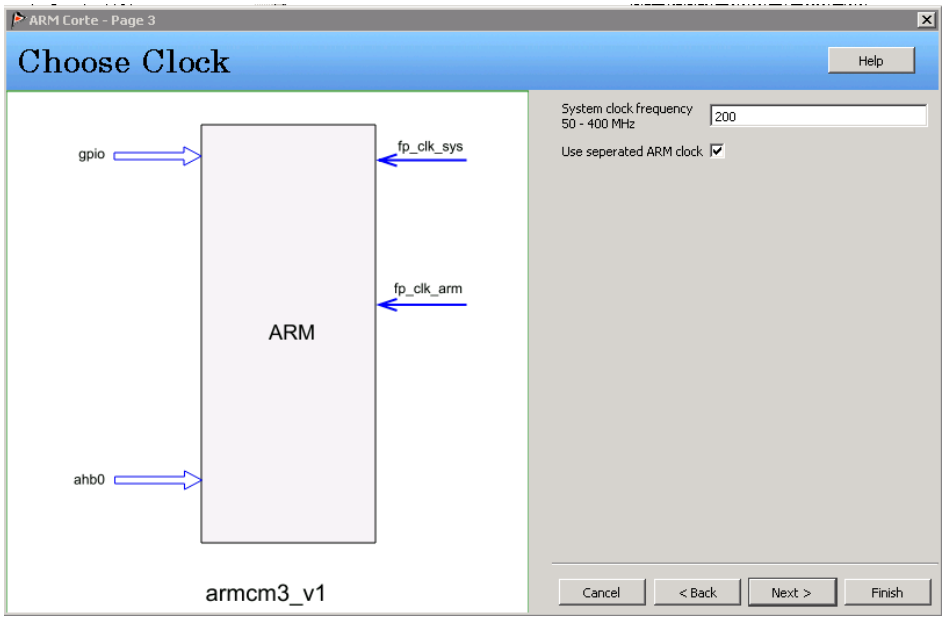

Figure 2-3(b) ***set clock***

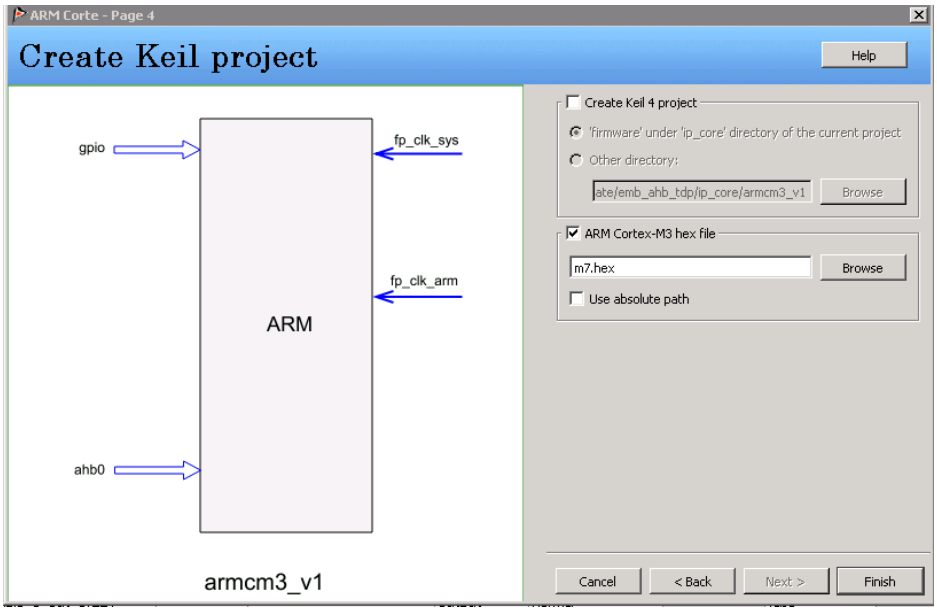

Figure 2-3(c) ***set hex file***

c) The c code in the firmware file "main.c" is used to achieve the function of accessing the EMB_AHB on the FPGA. The function flow is as figure 2-4.

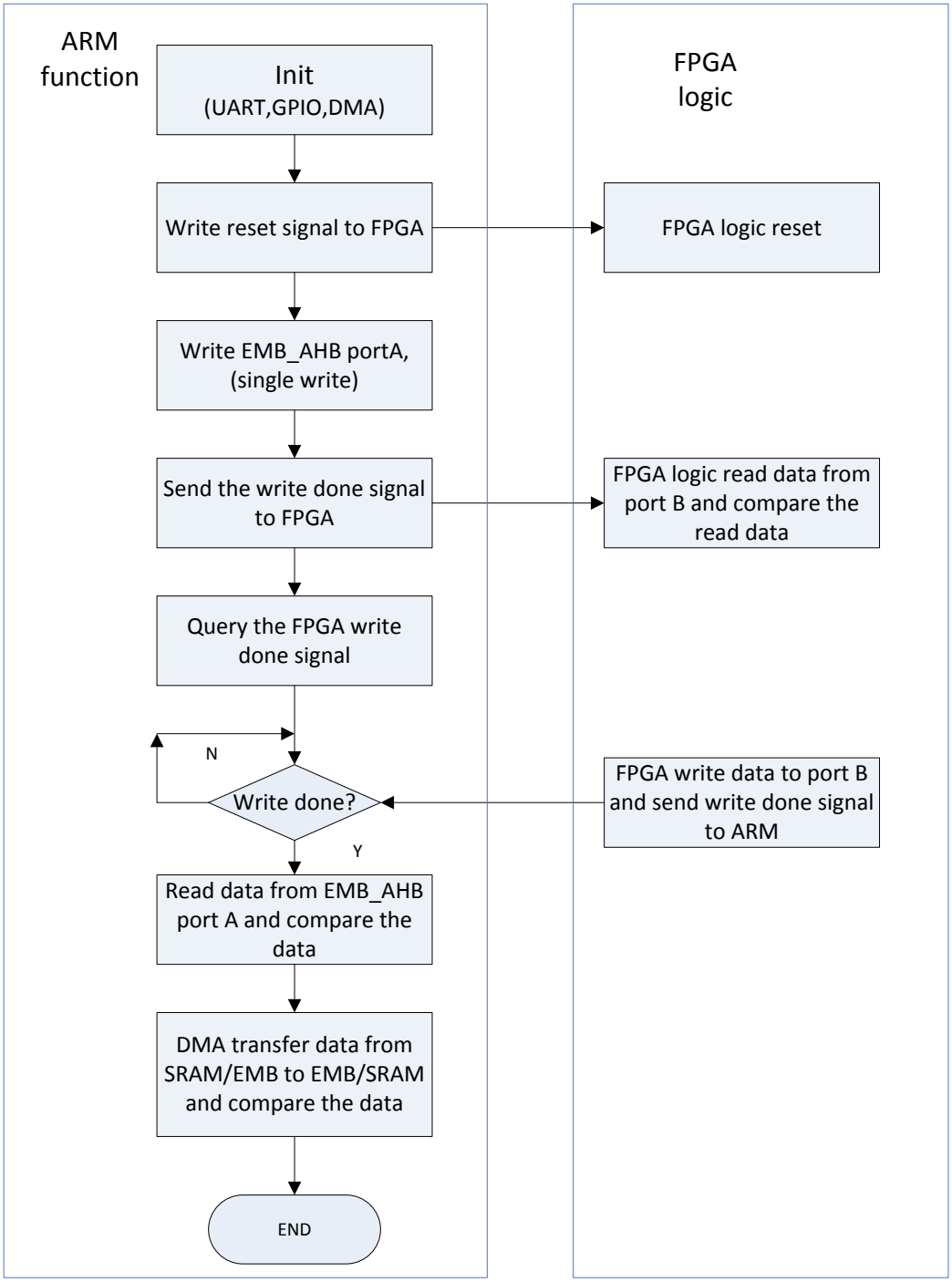

Figure 2-4 ***function flow***

3. EMB(tdp,512x32,generated by Wizard):

   a) This block is a 512 x 32bit memory with tdp mode and AHB interface, used as slave memory space.

   b) The ARM SOC provides two AHB interface, AHB0 and AHB1(as figure2-3(a)), which have different address space. In this example, AHB0_slave_interface is used to connect with the port A with interface. So, the Base Address can be configured as figure 2-5(a).

   c) The true dual port EMB has two kinds of interface; port A is of AHB interface, accessed by ARM,

port B is of memory interface, read/written by FPGA logic.

d) It is configured as the figure 2-5(a),2-5(b).

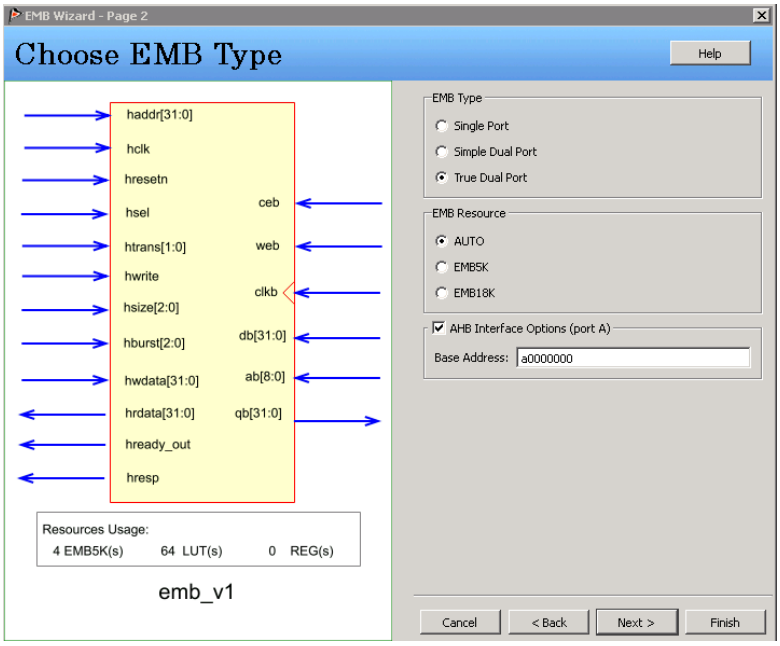

Figure 2-5(a) ***configure the EMB type***

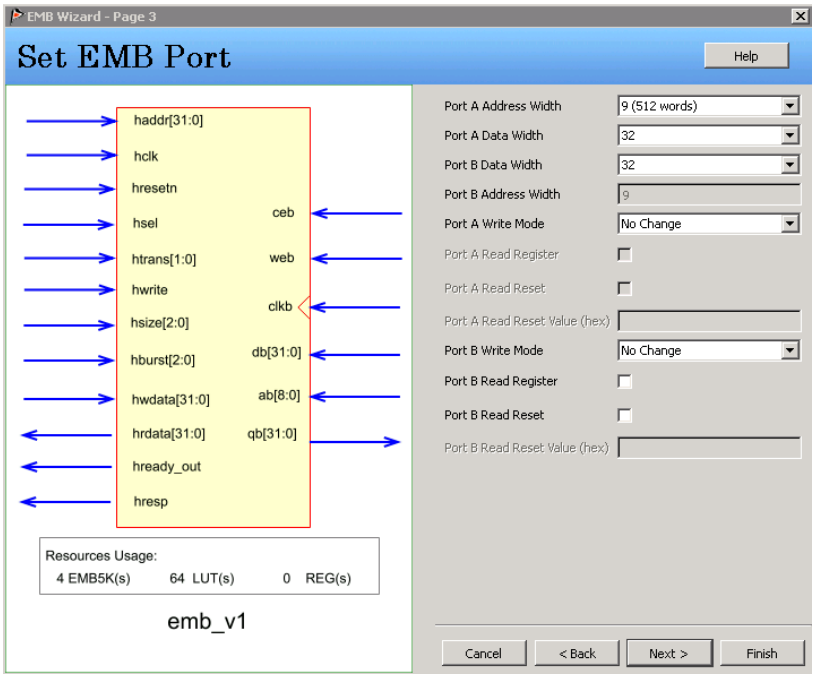

Figure 2-5(b) ***configure the EMB port***

4. FP logic(RTL design)

a) This part is used to access the port B of EMB.

b) The FPGA logic read data from EMB port B after receiving the write done signal sent by ARM and compare the read data, then, write data to port B and send the write done signal to ARM.

3 Example Result

The results can be displayed on the PC through serial port using the Tera Term tool which can be configured as figure 3-1 below. The results are shown in the figure 3-2.

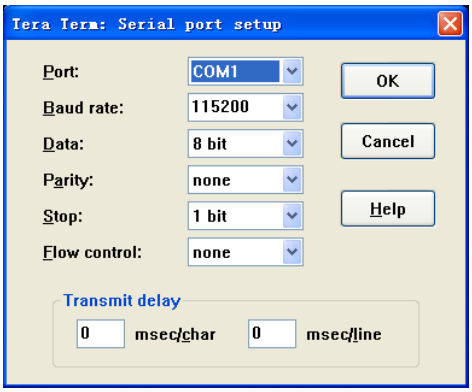

Figure 3-1 ***Tera Term configuration***

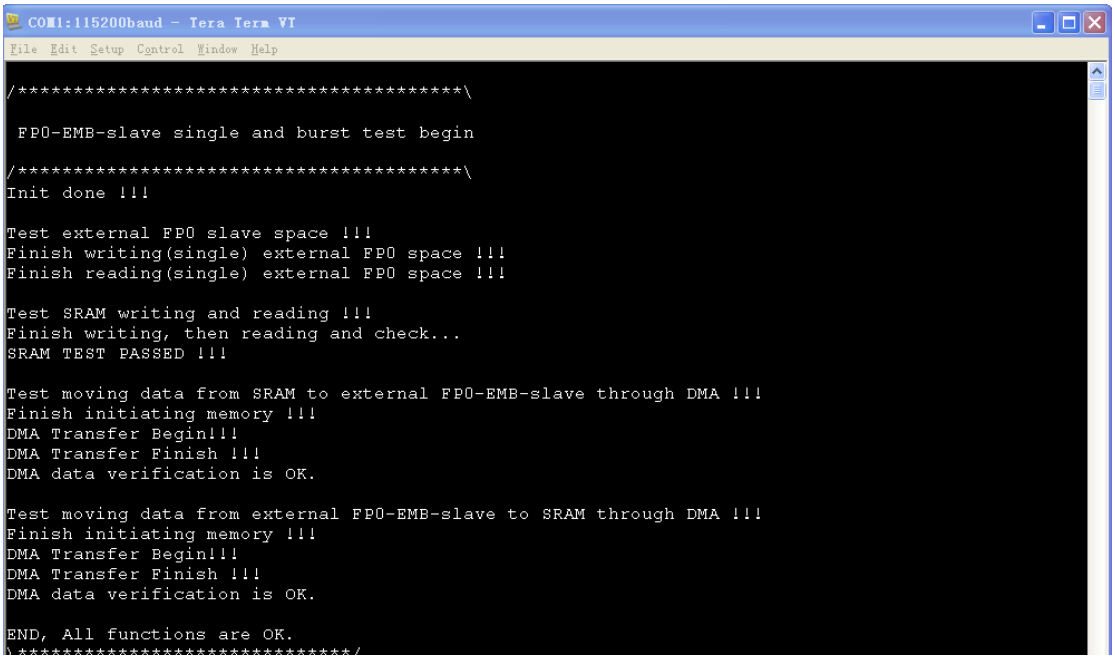

Figure 3-2 ***Example results***

4 Pin and Design Source description

4.1 Pin descriptions

Table 4-1 ***The EMB (tdp) with AHB interface example top module pin description***

Name	Direction	Width	Description
clk	Input	1	Clock input (20MHz)
rst_n	Input	1	Reset signal, low active
gpio_0_out_o	Output	32	GPIO output signal
led_rd_ok	Output	1	FPGA read port B done signal
led_wr_ok	Output	1	FPGA write port B done signal
Led_rd_wrong	Output	1	FPGA read data wrong signal

4.2 Pin assignments

The following figure4-1 shows the detail pin assignments in IO Editor of Primace

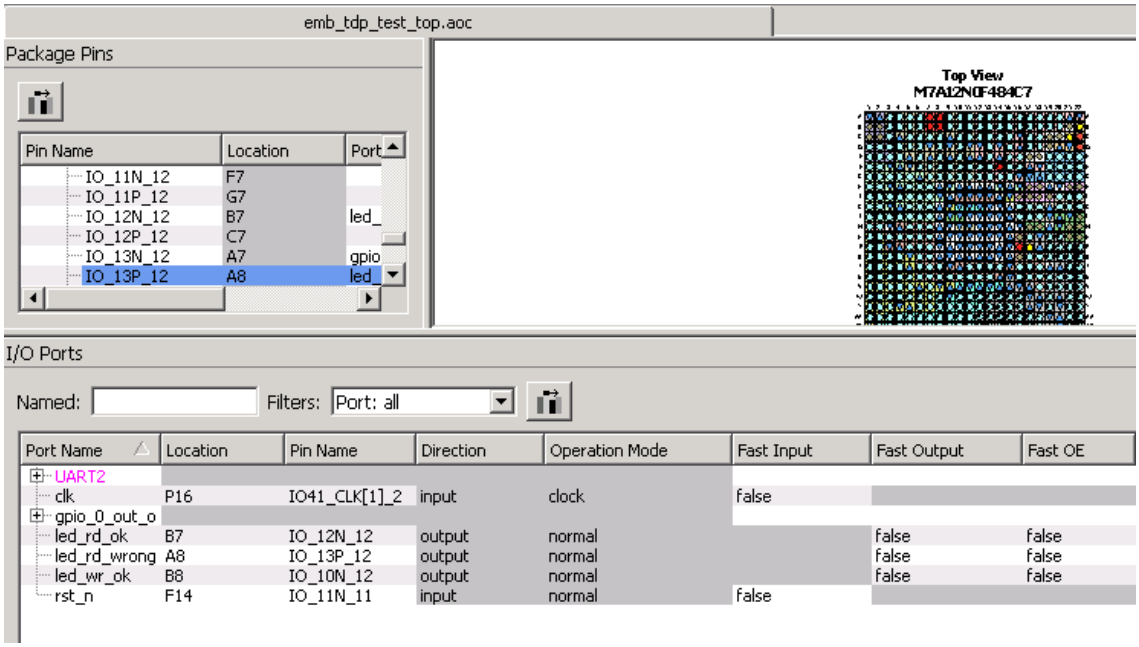

Figure 4-1 ***IO pin assignments***

4.3 Design source

The EMB(tdp) with AHB interface example RTL source files are shown in table 4-2.

Table 4-2 ***The EMB(tdp) with AHB interface example's source files description***

File	Description
RTL ./src/	./design/cme_ip_emb_ahb_v1_tdp
/ emb_tdp_test_top.v	The top module, implements the connection of all sub modules and write/read port B of EMB.
/ armcm3_v1.v	The ARM processor core implemented by ARM Wizard.
/ emb_v1.v	Ture duel port memory(512x32) implemented by EMB Wizard.
/pll_v1.v	Phase-locked loop, implemented by PLL Wizard.
Firmware	
/main.c	UART initiate, and access the EMB's port A on FPGA.

5 Revision History

Revision	Date	Comments
1.0	2013-11-18	Initial release